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SPECIFICATION

AN ANTIFUSE STRUCTURE AND A METHOD OF FORMING AN ANTIFUSE STRUCTURE

BACKGROUND

[0001] The present disclosure relates to antifuse structures and methods of forming antifuse structures, and in particular, to the use of hemispherical grained silicon or amorphous silicon as part of an inter-electrode dielectric in an antifuse.

[0002] FPGAs are known in the art. An FPGA comprises an interconnect routing architecture and programmable elements that may be programmed to selectively interconnect the logic modules to one another and to define the functions of the logic modules. To implement a particular circuit function, the circuit is mapped into the array and the appropriate programmable elements are programmed to implement the necessary wiring connections that form the user circuit.

[0003] An FPGA may also include other components, such as static random access memory (SRAM) blocks or dynamic random access memory (DRAM) arrays. Horizontal and vertical routing channels provide interconnections between the various components within an FPGA. Programmable connections are provided by programmable elements between the routing resources.

[0004] An FPGA can be programmed to implement virtually any set of digital functions by programming the programmable elements to implement the desired digital functions. There are several different types of programmable elements used in FPGAs, for example, MOS transistors and antifuse elements.

[0005] Antifuses may be used in FPGAs for programming purposes and as a mechanism for changing the operating mode. Antifuses may also be programmed to encode identification information about the FPGA, such as when the FPGA was fabricated. In addition, antifuses may be used as non-volatile programmable memory elements to store logic states in memories for row and column redundancy implementation. For example, antifuses for redundancy implementation on a DRAM are usually constructed in the same manner as the memory cell capacitors in a DRAM array. When programmed, an antifuse creates a short circuit or low resistance link, thereby enabling the particular redundant row, column or memory location.

[0006] FPGAs can contain hundreds to thousands of antifuses that may or may not need to be programmed. Therefore, it can take a large amount of time to program the antifuses in an FPGA. An unprogrammed antifuse essentially functions as a capacitor. For this reason, an antifuse having a reduced capacitance and low leakage, while maintaining low programming voltages would be beneficial.

[0007] However, improving the programming voltage on an antifuse (e.g., by decreasing the thickness of the dielectric or the size of the electrodes) can increase current leakage across the unprogrammed antifuse due to the smaller area occupied by it and thinner dielectric employed in it. Hence, an antifuse having a significantly reduced leakage current while maintaining reduced capacitance would also be beneficial.

SUMMARY

[0008] The present invention comprises an antifuse having a hemispherical grained (HSG) layer and a method of forming antifuse having a HSG layer. The antifuse of the present invention comprises a plurality of layers. A first layer comprises a lower electrode. A dielectric layer is disposed on the lower electrode, wherein the dielectric layer has a planar surface. A non-conductive HSG layer is

formed on the planar surface of the dielectric layer and an upper electrode is disposed on said non-conductive HSG layer forming the antifuse.

[0009] A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description of the invention and accompanying drawings, which set forth an illustrative embodiment in which the principles of the invention are utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Referring now to the figures, wherein like elements are numbered the same:

[0011] FIG. 1 is a simplified cross-sectional diagram of an antifuse;

[0012] FIG. 2 is a simplified graph illustrating the capacitance reduction ratio of the antifuse of FIG. 1;

[0013] FIG. 3 is a cross-sectional diagram illustrating the steps of forming a lower electrode, a dielectric layer, and an amorphous silicon layer on a substrate;

[0014] FIG. 4 is a cross-sectional diagram illustrating the steps of forming an amorphous silicon hemispherical grain layer on the layers of FIG. 3; and

[0015] FIG. 5 is a cross-sectional diagram illustrating the steps of forming an upper electrode layer on the layers of FIG. 4.

DETAILED DESCRIPTION

[0016] Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

[0017] In the present disclosure, Vcc is used to define the power supply for the digital circuit as designed. As one of ordinary skill in the art will readily recognize, the size of a digital circuit may vary greatly depending on a user's particular circuit requirements. Thus, the Vcc may change depending on the size of the circuit elements used.

[0018] FIG. 1 is a simplified cross-sectional diagram of an antifuse 10. Antifuse 10 includes a lower electrode 14 that is formed on an impurity region (not shown) in a semiconductor substrate 12. Lower electrode 14 can comprise a planar polysilicon layer formed on top of and in electrical contact with the impurity region. A dielectric element (or layer) 16 comprises a planar dielectric

layer 18 and a layer of hemispherical grained (HSG) amorphous polysilicon 20. Disposed on top of HSG amorphous polysilicon layer 20 is an upper electrode 22.

[0019] The antifuse 10 utilizes the HSG amorphous polysilicon layer 20 as part of the dielectric layer. The HSG amorphous polysilicon is typically referred to as "HSG amorphous poly" or "roughened amorphous poly". The HSG amorphous polysilicon layer 20 is a non-conductive polysilicon layer. The HSG amorphous polysilicon layer 20 may also be comprised of germanium (GE). Other materials contemplated include amorphous SiGe and amorphous SiC.

[0020] The HSG amorphous polysilicon layer 20 is disposed in a "rough state", that is, the resulting deposition of the HSG amorphous polysilicon layer 20 is uneven (i.e., generally not completely planar). By the nature of the "rough" surface of the HSG amorphous polysilicon layer 20, the thickness of dielectric element 16 is varied. The thickness of the dielectric element 16 can vary from about 100 Angstroms (Å) to about 300 Å. The thickness of the planar dielectric layer 18 is from about 5 Å to about 200 Å. The thickness of the HSG amorphous polysilicon layer 20 is from about 100 Å to about 500 Å.

[0021] An example of the possibility of having a varying degree of thicknesses is illustrated in FIG. 1. Arrow 24 illustrates one example of a thickness that is less than the thickness represented by arrow 26.

[0022] As those of ordinary skill in the art will readily recognize, the thickness of both the dielectric layer 18 and the HSG amorphous polysilicon layer 20 can vary depending on the desired circuit performance requirements. The above thicknesses are presented for illustrative purposes only and are not meant to limit the present disclosure.

[0023] By increasing the thickness of dielectric element 16 with HSG amorphous polysilicon layer 20, a reduced capacitance will result in the antifuse 10. This result is due to the capacitance being inversely proportional to the distance between the lower electrode 14 and the upper electrode 22. Depending on the thickness of dielectric element 16 at the program path (i.e., arrow 24, for illustrative purposes only), up to about 30% capacitance reduction can be achieved.

[0024] Current leakage may also be reduced as compared to prior art antifuses due to the reduced defect density. The defect density can be increased with a decrease in the dielectric layer. Due to the HSG layer, the average

thickness of the dielectric is increased and the effect of the defect on leakage current is decreased. The capacitance reduction is directly attributed to the portion of the dielectric element 16 represented by arrow 26, which is demonstrated in the following example:

[0025] The dielectric layer of the antifuse has a thickness of about 5 Å to about 200 Å, with a preferred thickness of about 20 Å to about 100 Å, and a more preferred thickness of about 40 Å to about 60 Å. The amorphous HSG layer has a thickness of about 100 Å to about 500 Å, with a preferred thickness of about 200 Å to about 400 Å, and a more preferred thickness of about 300 Å.

[0026] FIG. 2 is a simplified graph illustrating the estimated capacitance reduction ratio of the antifuse of FIG. 1. The estimated capacitance reduction ratio is based on known linear and triangular approximation theories used for calculating the thickness of dielectric element 16 having a HSG amorphous polysilicon layer 20, as illustrated in FIG. 1.

[0027] In addition, as one of ordinary skill in the art will recognize, when programming antifuse 10, the current will flow through dielectric element 16 at a thinner point, represented by arrow 24. Thus, the programming time is not affected by the increased thickness of the dielectric layer and reduced capacitance.

Moreover, the programming voltage is low due to the thinner point, represented by arrow 24. The antifuse can be programmed utilizing known methods.

[0028] FIGS. 3, 4, and 5 illustrate the steps of forming an antifuse. As illustrated in FIG. 3, a lower electrode 14 is formed on an impurity region (not shown) in a non-conductive semiconductor substrate 12. The lower electrode 14 may be formed of a planar polysilicon layer formed on top of and in electrical contact with an impurity region. The lower electrode 14 may also be formed of a planar metal layer, such as TiN, Ti, TaN, W, or TiW.

[0029] A planar dielectric layer 18 is disposed over the lower electrode 14. The dielectric layer 18 may be formed of a material such as silicon dioxide, silicon nitride, and the like. In some instances, the planar dielectric layer 18 may be omitted. In the preferred embodiment, an amorphous silicon layer 19 is deposited on the dielectric layer 18.

[0030] As illustrated in FIG. 4, a layer of HSG amorphous polysilicon 20 is then formed from the amorphous silicon layer 19 using a vacuum anneal process. A dielectric element 16 comprising the planar dielectric layer 18 and the HSG amorphous polysilicon layer 20 is formed.

[0031] The HSG may be formed on an amorphous carbon layer. The amorphous carbon layer can be doped with hydrogen, fluorine, or hydrogen and fluorine. The HSG amorphous carbon layer can be disposed between two layers of an adhesion-promoting material. In some cases, a dielectric layer may also be disposed with the HSG amorphous carbon layer between two layers of an adhesion-promoting material. Such an adhesion-promoting material can be SiC, SiN, and the like.

[0032] Generally, the dielectric element 16 can be formed using a fabrication method that comprises forming a layer of HSG amorphous polysilicon 20 on a dielectric layer 18 or, when a dielectric layer 18 is not utilized, on an impurity region or metal layer 14. Once the amorphous polysilicon layer 19 is deposited, the native oxide is removed. Finally, the amorphous polysilicon layer 19 is subjected to high-vacuum annealing and the HSG amorphous polysilicon layer 20 is formed. Other methods may be used to form HSG amorphous polysilicon layer 20, such as low-pressure chemical vapor deposition (LVCPD) and *in-situ* annealing under an ultrahigh vacuum.

[0033] As illustrated in FIG. 5, an upper electrode is disposed on the HSG amorphous polysilicon layer 20. The upper electrode 22 may be formed of a planar polysilicon layer formed on top of and in electrical contact with an impurity

region. The upper electrode 22 may also be formed of a planar metal layer, such as TiN, Ti, TaN, W, or TiW.

[0034] While embodiments and applications of this system have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

What is claimed is: